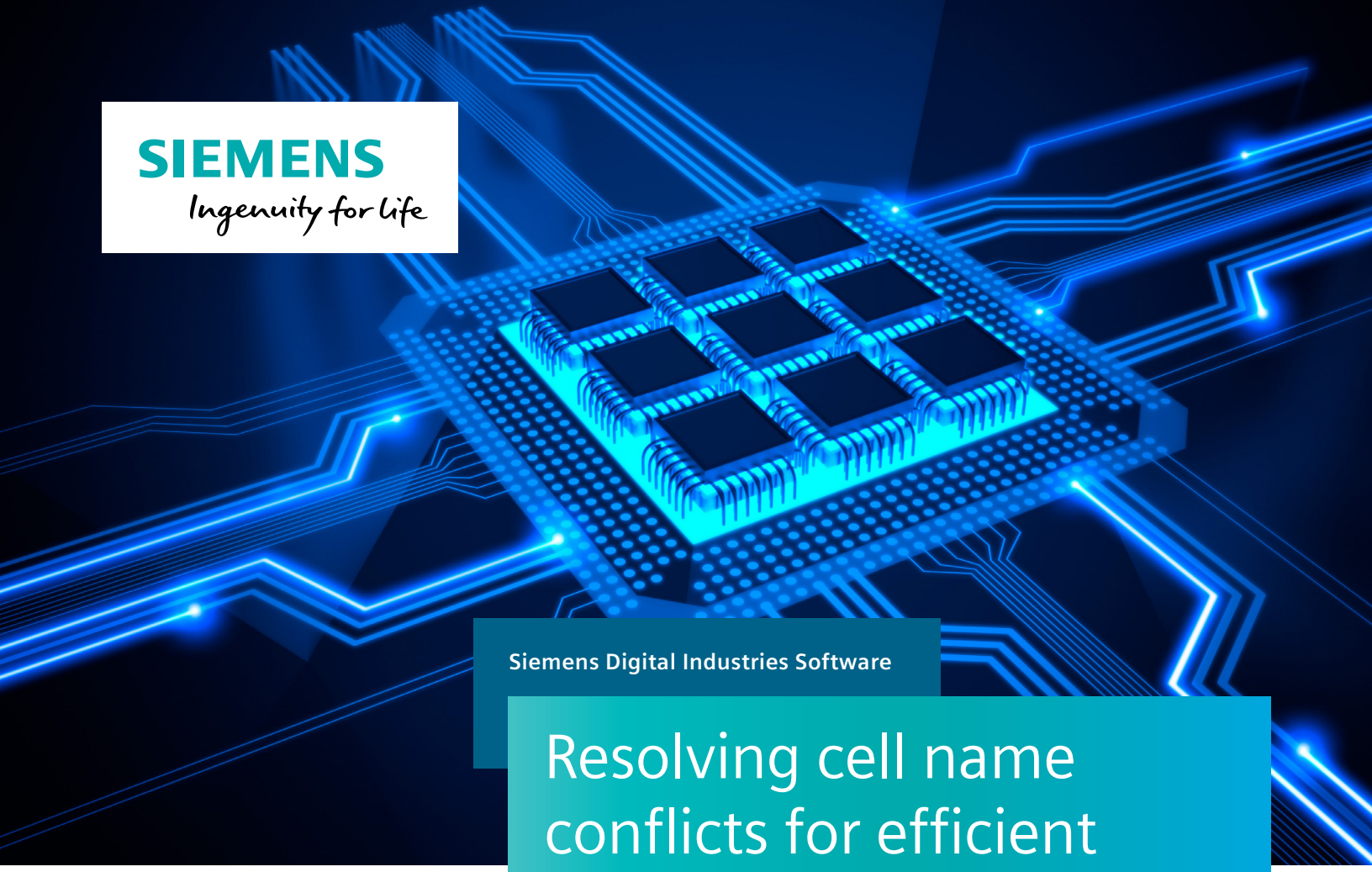

SIEMENS
Ingenuity for life

Siemens Digital Industries Software

Resolving cell name conflicts for efficient layout hierarchy

Executive summary

Duplicate cell names across multiple IP in an SoC can result in unexpected layout results at the full-chip level, larger file sizes, and the inability to run layout verification tools efficiently in hierarchical mode. The Calibre DESIGNrev tool provides a simple, efficient, automated solution for identifying, renaming, and reporting these cell name conflicts. The outcome is a clear and consistent design process, straightforward chip assembly, a clean and meaningful design hierarchy, faster EDA tool runtimes, and faster time to tapeout.

Dennis Joseph
Siemens EDA

Introduction

System-on-chip (SoC) designs are popular with consumers because they are at the core of smaller gadgets that cost less money and require less power. They are also popular with chip design teams, who can expedite time to market by incorporating reusable intellectual property (IP) blocks into multiple SoC designs. Design teams can either design and implement common functionality only once, or purchase fully verified IP from 3rd party suppliers. They can then focus on creating the proprietary IP that differentiates their designs, reducing the number of tasks needed to design an SoC while meeting ambitious delivery schedules.

Although working with multiple IP suppliers has its advantages, it also creates its own set of challenges for successful integration of 3rd party content. The suppliers will have individually verified their IP at the block level, but design teams must still successfully merge and verify all the IP at the full-chip level. One constant challenge in this process is the presence of duplicate cell names across IPs.

If not handled correctly, these cell name conflicts among 3rd party IP blocks can result in a number of undesirable outcomes, such as unexpected layout results at the full-chip level, larger file sizes, and the inability to run layout verification tools efficiently in hierarchical mode. Managing and resolving cell name conflicts is an essential part of an efficient and accurate design flow.

Cell name conflicts

If they aren't correctly managed, cell name conflicts can cause unpredictable output in an assembled full-chip layout. If the designer is not careful, layout merge tools may not create the expected layout, as it may not be obvious which version of the conflicting cells was written to the output (figure 1).

Physical verification and circuit verification tools then accept and use the incorrect data, run for hours, and generate meaningless error results. Worse yet, it may not be obvious why the results are meaningless, or even that they are. The time and resources required to analyze and resolve this situation are completely wasted and unnecessarily impact tapeout schedules.

Design teams may choose to uniquely rename all cells in all input layouts prior to merging, simply eliminating all cell name conflicts (figure 2). While this method works, it unnecessarily increases the merged layout's file size, especially if there is duplicate content among the cells with name conflicts. Renaming also typically increases the time required for verification tasks, as the layouts may no longer utilize the hierarchical efficiency of the original design.

Fortunately, the Calibre® DESIGNrev™ FileMerge functionality provides a fast and efficient solution that can help design teams quickly and accurately resolve cell name conflicts. It can also report all the cell name conflicts, which allows design teams to review discrepancies, follow up with their IP suppliers as needed, and rename cell name conflicts prior to merging for the best results.

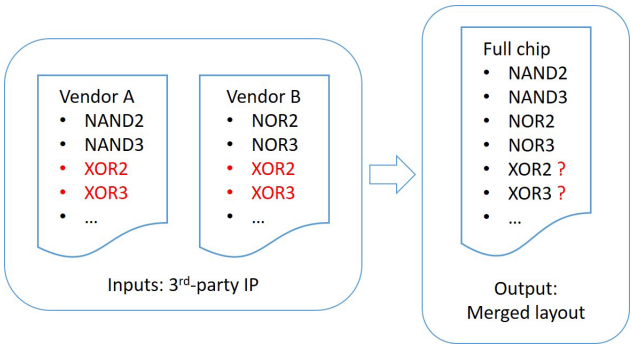

Figure 1: Both vendors provided IP named XOR2 and XOR3. It may not be clear to a designer which version of those two cell conflicts were written to the output.

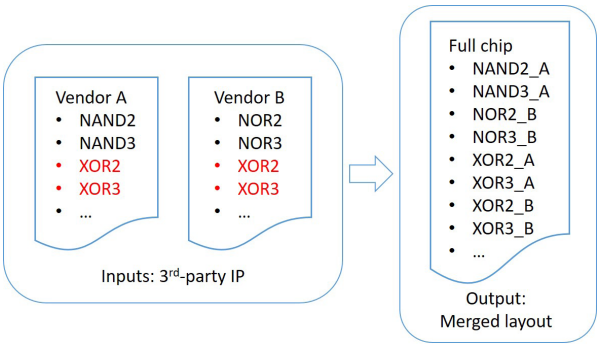

Figure 2: Renaming all cells removes all conflicts, but can increase file size and verification runtimes.

Calibre DESIGNrev FileMerge

The Calibre DESIGNrev FileMerge functionality provides several levels of cell conflict management that allows design teams to create customized flows that deliver the level of detail they require.

Renaming cell conflicts during merge

Designers can rename all the conflicting cells by invoking the FileMerge functionality in its rename mode from the command line:

>> calibredrv -a layout filemerge -in fullchip.oas -in vendor_a.oas -in vendor_b.oas ... **-mode rename** -out fullchip_merged.oas

With the rename option, the output retains the original name of the first occurrence of a cell name conflict, renaming subsequent versions. Designers may choose a custom prefix or suffix to use when renaming cells to get a more meaningful name in the merged layout. Renaming only the conflicting cells reduces the number of renamed cells in the layout (figure 3).

However, this option still results in a layout file that is larger than needed, since some of the renamed cells may have duplicate contents. Also, the source of a particular cell may still not be clear to the designer.

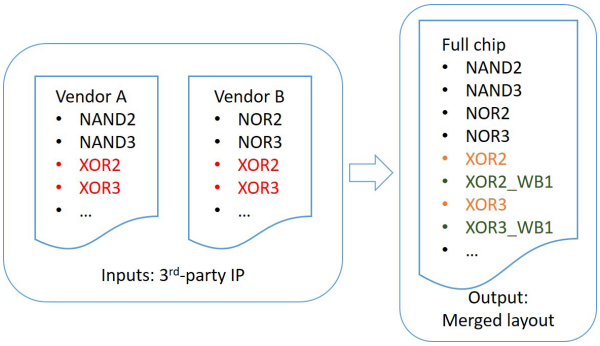

Figure 3: The Calibre DESIGNrev FileMerge functionality lets designers quickly rename only conflicting cells.

With the rename option, the output retains the original name of the first occurrence of a cell name conflict, renaming subsequent versions. Designers may choose a custom prefix or suffix to use when renaming cells to get a more meaningful name in the merged layout. Renaming only the conflicting cells reduces the number of renamed cells in the layout (figure 3).

However, this option still results in a layout file that is larger than needed, since some of the renamed cells may have duplicate contents. Also, the source of a particular cell may still not be clear to the designer.

Comparing cell contents when resolving cell conflicts

To rename only those cells that have different contents, designers can add the -smartdiff option to the FileMerge command. This option compares the cell contents of each cell conflict and renames only the conflicts where the contents differ.

With the smartdiff content comparison enabled, the FileMerge functionality will only rename and report cells with actual content differences (figure 4).

>> calibredrv -a layout filemerge -in fullchip.oas -in vendor_a.oas -in vendor_b.oas ... -mode rename -out fullchip_merged.oas **-smartdiff**

The -smartdiff option also supports additional options to ignore texts, ignore properties, and to convert paths to polygons. These options provide designers with very precise control of what is reported as a difference, allowing them to develop a customized flow that ensures unique cell names are used only when they are truly needed. This smart renaming capability ensures faster Calibre runtimes downstream, because the hierarchical Calibre engine runs faster when it has fewer cells to process in a design.

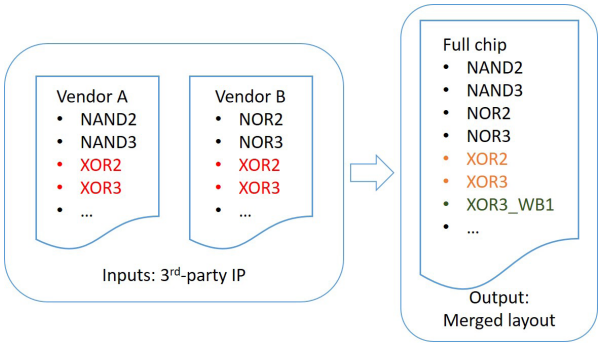

Figure 4: Adding the -smartdiff option ensures that only conflicting cells with actual differences in content are renamed. The contents of XOR2 are the same from both IP vendors, but the contents of XOR3 differ, so the second XOR3 cell is renamed.

Cell conflict output

When designers review the FileMerge output, the origin of the newly renamed cells may not always be obvious. Even when designers specify a custom prefix or suffix, one version of the cells in conflict keeps the original name. Without knowing which cells from which input layouts were renamed, and what those new names are in the output, design teams may not have enough insight to evaluate the output and know that it contains what they expect. A report of all the cell conflicts helps provide this detail, and allows design teams to follow up with their IP suppliers in the event of any discrepancies. With this information in hand, design teams can ensure that the merged output contains everything they expect.

Reporting renamed cells during merge

Adding the -reportconflicts option to the FileMerge functionality lists all the cell name conflicts in the transcript. This option can be combined with the -smartdiff option to get the list of cell name conflicts where the content differs:

```
>> calibredrv -a layout filemerge -in fullchip.oas -in vendor_a.oas -in vendor_b.oas ... -mode rename -out fullchip_
merged.oas -reportconflicts -smartdiff
```

The conflicts and the new names assigned in the merge (Figure 3) are reported in the output:

```
Note: cell XOR3 already exists in vendor_a.oas and content differs, renamed with XOR3_WB1 from vendor_b.oas.
```

Using this report, designers can confirm that the output contains everything that is expected, and follow up with their IP suppliers regarding any discrepancies. They can also this information to update the hierarchical cell list to ensure a fast and accurate layout vs. schematic (LVS) run.

Reporting cell conflicts without merging

Design teams sometimes need conflict information to review their 3rd party IP. Because this type of review usually occurs near the beginning of a project, when actually merging the layout may not create meaningful output, design teams can save time by using the FileMerge functionality to just get the list of conflicts, without actually writing the merged layout. Again,

this option can be combined with the -smartdiff option to list only the cell name conflicts in which the contents differ.

The reportconflictsonly mode reports all the same information as the -reportconflicts option, with the exception of any renamed cell names, since there is no output layout created. With this information in hand, design teams can follow up with their IP suppliers regarding any unexpected conflicts. They can also use this information to rename the cell name conflicts prior to merging, so that only the cell name conflicts where the content differs are renamed in the output layout. (figure 5).

>> calibredrv -a layout filemerge -in fullchip.oas -in vendor_a.oas -in vendor_b.oas ... **-mode reportconflictsonly** -smartdiff

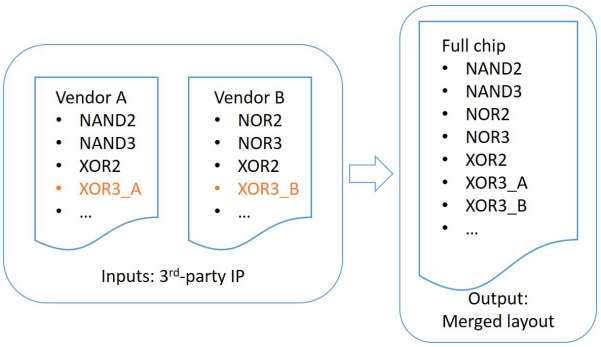

Figure 5: Renaming only cell name conflicts where the content differs prior to merging creates an output layout that clearly indicates the source of the content, maintains hierarchical efficiency, and minimizes file size.

Conclusion

When design teams work with multiple 3rd party IP suppliers, they often encounter duplicate cell names across multiple IP. These cell name conflicts must be managed across all external IP to avoid generating meaningless verification results that waste time, frustrate designers, and impact tapeout schedules. Simply renaming all cells in 3rd party IP can cause downstream issues during physical and circuit verification. The best solution is to identify all cell name conflicts, analyze cell contents to identify true differences, and meaningfully rename only the cell name conflicts with content differences.

Multiple reporting options let teams identify the origins of the cell conflicts to confirm that the merged output is what they expected. This information also allows them to follow up with IP suppliers regarding any discrepancies. They can also use this detail to rename selected cell name conflicts prior to merging to get the clearest, most efficient layout.

For all these situations, the Calibre DESIGNrev FileMerge functionality offers a simple, efficient, automated solution for identifying, renaming, and reporting these cell conflicts. The outcome is a clear design process, straightforward chip assembly, a clean and meaningful design hierarchy, faster EDA tool runtimes, and faster time to tapeout.

Siemens Digital Industries Software

Headquarters
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 972 987 3000

Americas
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 314 264 8499

Europe
Stephenson House
Sir William Siemens Square
Frimley, Camberley
Surrey, GU16 8QD
+44 (0) 1276 413200

Asia-Pacific
Unit 901-902, 9/F
Tower B, Manulife Financial Centre
223-231 Wai Yip Street, Kwun Tong
Kowloon, Hong Kong
+852 2230 3333

About Siemens Digital Industries Software

Siemens Digital Industries Software is driving transformation to enable a digital enterprise where engineering, manufacturing and electronics design meet tomorrow. The Xcelerator portfolio helps companies of all sizes create and leverage digital twins that provide organizations with new insights, opportunities and levels of automation to drive innovation. For more information on Siemens Digital Industries Software products and services, visit siemens.com/software or follow us on LinkedIn, Twitter, Facebook and Instagram. Siemens Digital Industries Software – Where today meets tomorrow.

siemens.com/eda

82574-C2 10/20 A