DIGITAL INDUSTRIES SOFTWARE

How PCB designers can use IPC specifications for DFM

Executive summary
IPC Documentation covers hundreds of specifications designed to improve the overall reliability of a PCB throughout its product lifecycle. The specifications and classes developed by IPC are ubiquitous across the industry and form the de facto standards adopted by many organizations. When setting up a DFM ruleset many are tempted to simply adopt these IPC standards as a basis for their DFM process and allow these constraints to drive the quality of their product. This line of thought is pervasive throughout the industry but represents a fundamental misunderstanding of how IPC specifications relate to DFM Rules.

SIEMENS

Introduction

The first thing that comes to mind when people think about PCB design and quality is inevitably IPC specifications, a series of hundreds of industry standard documents which cover multiple stages of the electronics product development cycle. IPC specifications categorize PCBs into "performance classes." These classes are so commonly known to PCB designers and manufacturers, as well as companies that incorporate PCBs into their products, that just noting a class range provides general understanding of the overall type of work that the PCB is intended for. Class 1 represents general off the shelf electronic products, such as the PCB inside a washing machine that costs $5 to build. Class 2 boards are built for dedicated service, and Class 3 are for high reliability or harsh operating environment electronic products, with tight tolerances, multiple layers, and refined electronics.

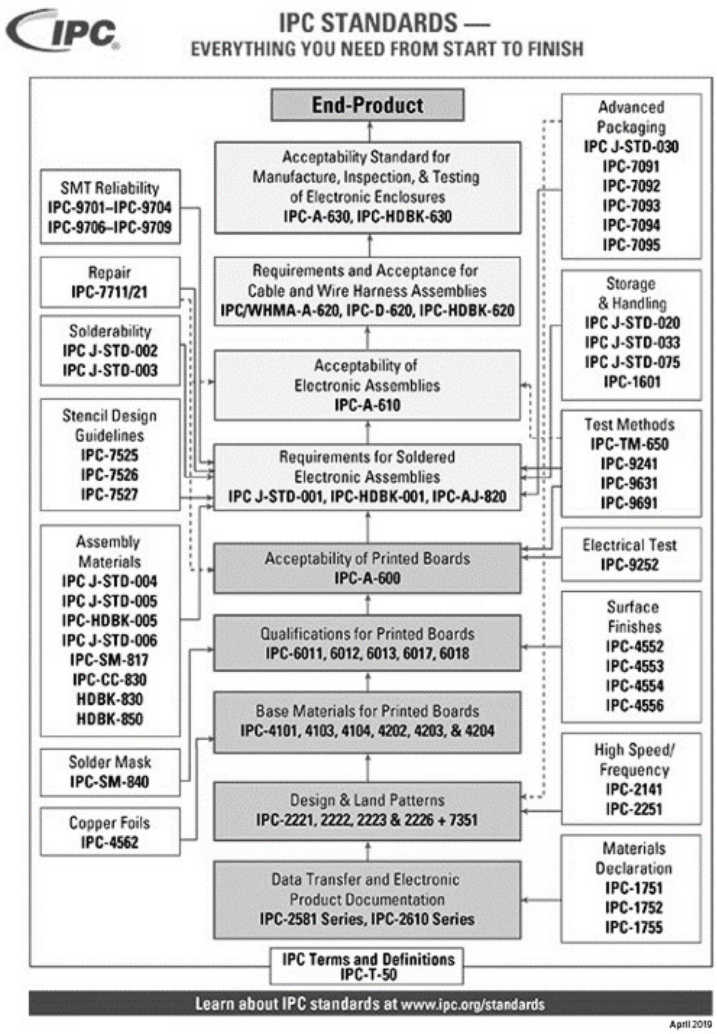

Figure 1. All the IPC standards that apply to designing and building a PCB.
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In addition to classes, IPC standards also delineate producibility levels for the density of the design being created. Level A is for general producibility, Level B is for standard producibility, and Level C is for high design producibility. We will explore the specifications behind these classes and levels and how we can leverage this information into a design for manufacturing (DFM) ruleset.

For DFM, designers often refer to the IPC standards and ask how to include them in their EDA design rule checks (DRC) list, ideally through a plug-and-play solution that will result in a board design which automatically conforms to the required class. However, the reality of implementing these specifications is not so simple. In some cases, it's done automatically by a DFM tool and sometimes not.

Figure 1 shows each specification that corresponds to the steps within the process of building a board, from documentation to the end product. Each step has several substeps associated with it. Understanding where each of these specifications applies to steps in the process helps isolate the ones specifically relevant to DFM.

Acceptability and quality

Acceptability of printer boards IPC-A-600

2.0 Externally Observable Characteristics
This section addresses those characteristics which are observable from the surface. This includes those characteristics that are external and internal in the printed board but visible from the surface as follows:

- **Surface imperfections** such as burrs, nicks, scratches, gouges, cut fibers, weave exposure and voids
- **Subsurface imperfections** such as foreign inclusions, measling/crazing, delamination, pink ring and laminate voids
- **Imperfections in conductive pattern** such as loss of adhesion, reduction of conductor width or thickness due to nicks, pinholes, scratches, surface plating or coating defects
- **Hole characteristics** such as diameter, misregistration, foreign material, and plating or coating defects
- **Marking anomalies** including location, size, readability, and accuracy
- **Solder resist surface coating imperfections** such as misregistration, blisters, bubbles, delamination, adhesion, physical damage and thickness
- **Dimensional characteristics** including printed board size and thickness, hole size and pattern accuracy, conductor width and spacing, registration and annular ring

Figure 2. Section 2 in IPC 600.

IPC specifications are focused on product acceptability and quality. What is meant by acceptability? Those that are specifically named as acceptability standards directly reflect the quality of the board when it comes out of the assembly and fabrication processes.

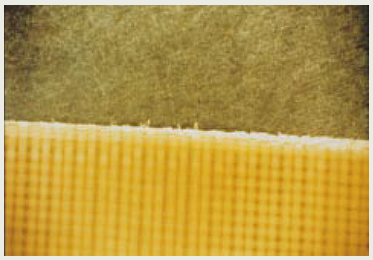
IPC-A-600 is a specification that designers often ask if they should adopt into a DFM ruleset, but this is a common misconception. *IPC-A-600* is an acceptability specification that represents a set of conditions that dictate the overall quality of the finished product, but it is not a design standard. This quality is determined by numerous external sources and environments typically present during fabrication of the PCB.

For example, Figure 2 details one of the first sections of the specifications: Section 2.0 Externally Observable Characteristics. This section addresses imperfections related to the surface and subsurface conductive patterns, hole characteristics, resisting surface coating, dimensional characteristics, and others. These acceptability characteristics represent imperfections in the final product that can result from the manufacturing process. They do not represent characteristics or imperfections within the digital data provided to manufacturing; thus, designers do not need to be concerned with them.

For example, measling and crazing occurs when air pockets are trapped between resin layers. If this pocket is drilled and plated, the hole becomes filled with copper. These air pockets are a result of older resin being used during production, or prepregs not being properly stored in a dry environment. Your fabricator using older resins or storing materials at an improper humidity level is not something a designer could, or even should, consider. Meazling and crazing issues would only be identified by incoming inspection and not something that could be designed out.

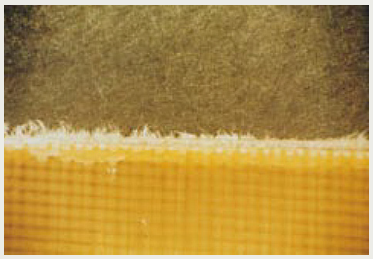
Target condition – Class 1,2,3

- Edge conditions – smooth, no burrs



Acceptable – Class 1,2,3

- Edge conditions – rough but not frayed

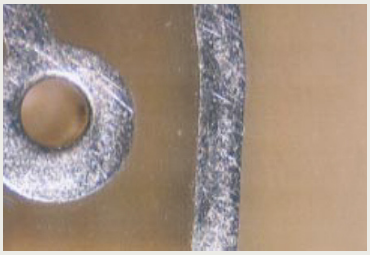


Nonconforming – Class 1,2,3

- Edge conditions – frayed with loose burrs
- Edge conditions – burrs affect fit and function

Figure 3. Nonmetallic burs are representative of the quality of the depanelization process (*IPC-A-600K Section 2.1.1.1 Nonmetallic Burs*). These images are used as an example of acceptable final appearance and separate the quality into groups showing what is acceptable and what is nonconforming based on class 1, 2 or 3. This quality depends on the upkeep of the machinery used by the fab house. (Copyright IPC-A-600 reprinted with permission)

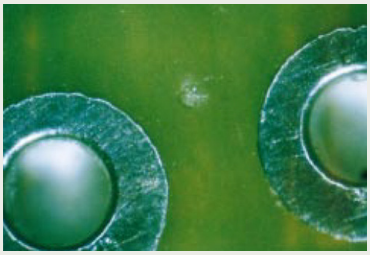
Other characteristics, such as scratches, nicks and surface defects, can exist within the original materials, while surface defects can result from human error such as a thumbprint from mistakenly mishandling a board. Those are process issues, not design issues.



Target condition – Class 1,2,3

- Edge conditions – smooth, no burrs

Figure 4. An example of an acceptable target condition, with a smooth surface appearance *IPC-A-600K Section 2.1.2 Nicks*. (Copyright IPC-A-600 reprinted with permission)



Nonconforming – Class 1,2,3

- Pits or voids larger than 0.8mm [0.031 in]
- Total board area affected exceeds 5 percent on either side
- Pits or voids bridge conductors

Figure 5. An example of a non-conforming board showing visible pitting between the two vias that is larger than 0.8 mm (*IPC-A-600K Pits and Voids*). (Copyright IPC-A-600 reprinted with permission)

These conditions cannot be specified on the data provided to the PCB fabrication house; it would be impossible to define rules of this nature within a DRC or a DFM constraint.

Some specifications focus on materials. Both the Base Materials for Printed Boards (*IPC-4101 series*) for fabricators and Assembly Materials (*IPC J-STD-004, IPC J-STD-005, IPC-HDBK-005, IPC J-STD-006, IPC-SM-817, IPC-CC-830, HDBK-830 and HDBK-850*) for assemblers mention materials and components used within a board.

Still other specifications deal exclusively with the storage and handling of the product, surface finishes and various other production quality situations.

Looking at these specifications as a whole, while useful and insightful, it quickly becomes apparent that they are built around acceptability and quality of the resulting product. These specs are not intended to define the limits of what can be manufactured and definitely are not meant to be design specifications.

What design issues can lead to a lower quality product?

Some design decisions can lead to a higher possibility of solder paste issues, but these conditions and values are not outlined in any IPC standard, rather they must be incorporated independently as part of a rigorous DFM ruleset put in place.

Which IPC specifications are useful as quantifiable design rules?

After removing acceptability and quality standards from consideration, only a small percentage of the IPC specifications can be usefully incorporated into EDA DRCs or DFM rules. These are mainly within the Design and Land Patterns specification. Within this area, the *IPC-2220* series applies to through-hole technology and *IPC-7351* applies to surface mount designs.

IPC-2220 series

IPC 2221 is a generic standard for printed board design providing standards and specifications that cover layout, material selection and general thermal and voltage requirements. Many of the specifications listed within this standard can be adapted to create DFM rulesets. A good example of this would be *IPC-2221 4.6.1.2 Mask Clearance and Dams* (Figure 6).

Table 4-16. Typical minimum solder mask clearances and dams

Mask type	Clearance
Liquid Screenable	0.25 mm [0.10 in]
Photo imageable Dry Film	0.051 mm [0.002 in]
LPI	0.051 mm [0.002 in]

Figure 6. Mask clearances and dams should be in accordance with Table 4-16 in the IPC-2221 specification. Clear areas may have to be provided for assembly fiducials (*IPC-2221 4.6.1.2 Mask Clearance and Dams*).

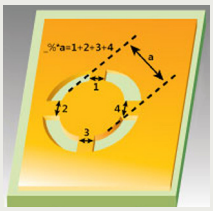
The table in Figure 6 shows that the mask and fiducial clearances have been separated by different mask types: liquid screenable, photo-imageable dry film and liquid photo imageable (LPI). These clearance values can be added to a DFM ruleset for each of these mask types: 250 microns to screen print, 51 microns for dry film, and 51 microns for LPI. This example indicates that, despite the knowledge of IPC design specifications, it is still necessary to know the manufacturing process of the PCB fabricators.

Another example of an important check that can be utilized with your DFM tool is *IPC-2222 9.1.2 Thermal Relief in Conductor Plans*. This check specifies that the total thermal tie cross-section area, including connections on the multiple planes, need to meet the ”60-percent rule” to provide successful thermal relief during assembly. This means dividing 60 percent of the land area to be thermal relieved by the number of webs to obtain the proper width of each web. This relationship between the hole size, land and web area is critical to provide successful thermal relief during printed board assembly. The total thermal tie cross-sectional area including connections on multiple planes need to meet the minimum current carrying capacity requirements for a given net but still allow the solder to properly wick for all thermal pads and plated through holes.

Additionally, a good DFM and or EDA DRC tool should also identify these thermal pads and holes to look for starvation to insure there is enough copper connection to meet the electrical requirements of the circuit. To create a useful DFM rule, set the web connections value to 60 percent within your DFM ruleset.

Thermal spoke connection (percentage)

Successful thermal relief during PCB assembly is dependent on the correct correlation between sizes of lands and their thermal spokes. According to IPC-2222A (2010-December) standard, a ratio of 60 percent should be maintained between the combined spoke width and the land diameter. Thermal spoke connection (percentage) reports combined spoke width versus land diameter ratios smaller than the threshold value (recommended 60 percent) which could indicate insufficient thermal relief during assembly. The constraint is applicable to positive layers only and reports only thermal pads for PTH.



A good example of how a designer might setup such a rule in a DFM tool like Valor NPI is utilizing the "Thermal spoke connection (percentage)" check for pin through holes.

Performance classes in IPC 2221

As previously mentioned, the IPC specifications describe performance classes (1, 2 and 3) and producibility levels (A, B and C). *IPC 2221 section 9.1.2* states that an annular ring is required for all plated through-holes in a Class 3 design. For Class 1 and Class 2 products, a partial or whole breakout is allowed. It also states that the annular rings must meet the requirements per Table 9-2 shown in Figure 7 and that all classes must have 25 microns for internal supported holes and 50 microns for external supported holes. As well in this case, the knowledge of the manufacturing capabilities of the PCB fabricator would be beneficial to define the correct values.

Annular ring	Class 1, 2 and 3
Internal supported	25.0 microns [0.000984 in]
External supported	50.0 microns [0.00197 in]

Figure 7. Annular rings requirement table (*IPC-2221 9.1.2 Annular Ring Requirements Table 9-2*).

In this instance, the constraint value requirement for these different classes is the same. Break out would never appear when analyzing digital data, but a designer can help prevent breakout for Class 3 by setting a high reliability classification value, up from the 25 microns default to maybe 35 for internal, and from 50 to the 75 for external. However, this is a judgement call to ensure the end product meets the specification, and it is not a value adapted from the IPC specification.

Another approach might be to consider adding teardrops to the design because they provide additional area to help prevent breakout (Figure 8).

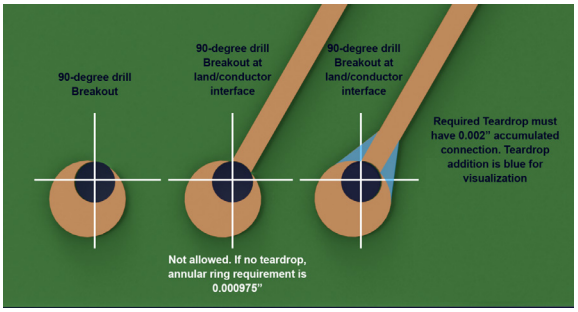


Figure 8. Adding teardrops in the design can help prevent break out.

Trace widths and IPC 2221

IPC 2221 section 10.1.1 provides minimum conductor widths. It states the thickness and the width of conductors on the finished printed board should be determined based on the signal characteristics, current carrying requirement and maximum allowable temperature rise.

As there is no single trace width (nor line spacing) that can be applied universally for all signal frequencies and impedances, designers typically work with their fabricators to determine the best trace widths and spacings to use for a design. There is nothing from the IPC-221 specification to apply to DFM in this case.

IPC-7351

For IPC-7351 surface mount design and land patterns specifications, Siemens Valor NPI DFM solution includes these values in its default settings.

If a designer creates a new classification set, the tool automatically adds the constraints associated with this specification into the new classification set. Of course, any of these values can be overridden based on the assembly partners guidelines.

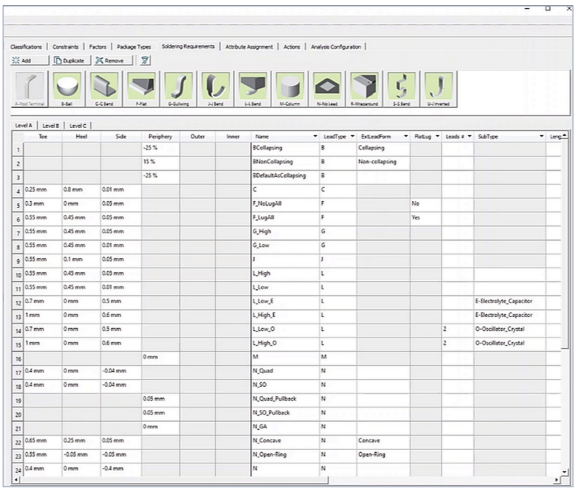


Figure 9. PC-7351 surface mount design and land pattern standard is supported and imported directly into Valor NPIs Analysis Definition Manager. Any of these values or pin types can be changed and customized for any classification sets.

The assembler may have experience with a certain package that can be improved if the solder validation rules are different than what IPC-7351 calls for. The producibility levels mentioned previously also are applicable here.

Setting up classifications in the DFM software

How these standards are deployed can look different depending on a designer's DFM practices and workflow. The ideal methodology is to leverage a manufacturing-driven design approach, which means letting the manufacturing constraints drive the PCB design constraints.

Valor NPI software's Analysis Definition Manager (ADM) defines the DFM constraints in an intuitive, hierarchical table. Within the ADM, a designer can define and name unlimited classification sets. For example, one could be defined and labeled as "Standard Technology." For this classification set, you might set IPC-7351, so then class B rules could be applied. For another technology classification of products, one might set class C rules to be applied and the classification defined as "Advanced Technology."

Furthermore, factors or criteria can be used to identify which designs should fall under "Standard Technology" and which ones should be designated "Advanced Technology." The factors could be layer count, copper weight, aspect ratio or the use of sequential lamination. Defining this criteria allows the Valor NPI software to automatically select the correct DFM ruleset to apply to a given design. This eliminates the risk of a design being mistakenly checked against the wrong ruleset.

When a design is loaded into Valor NPI, the software assesses which classification set to apply. It does this by sampling the data and capturing the values associated with the factors selected for assigning the classification sets. If a design specifies trace widths less than 4 mils and is classified as "Advanced Technology," when the design opened in Valor NPI has 3 mil traces, the software will automatically run the DFM rule set for "Advanced Technology." Valor NPI also has a few technology detections that determine if certain DFM checks need to be run. For example, if the software sees that the aspect ratio meets the IPC definition for microvia technology of less than or equal to 1.0 and the via depth is less than 9.84 mils, then microvia DFM checks are automatically run. Similar automation exists for other technologies such as HDI and rigid-flex circuits.

Conclusion

This is just a few examples of how to look at using IPC specifications for PCB designs. The majority of requirements might not be useful for a designer who is creating DFM or DRC rulesets. Valor NPI helps to take the guesswork out of applying IPC rules that relate to PCB design data for DFM with the aim to save designers' time they would otherwise have to spend on research.

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